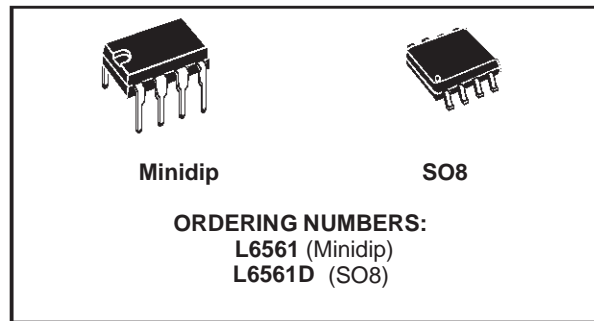


## POWER FACTOR CORRECTOR

- VERY PRECISE ADJUSTABLE OUTPUT
- OVERVOLTAGE PROTECTION
- MICROPOWER START-UP CURRENT (50µA TYP.)
- VERY LOW OPERATING SUPPLY CURRENT (4mA TYP.)
- INTERNAL START-UP TIMER
- CURRENT SENSE FILTER ON CHIP
- DISABLE FUNCTION
- 1% PRECISION (@  $T_j = 25^\circ\text{C}$ ) INTERNAL REFERENCE VOLTAGE
- TRANSITION MODE OPERATION
- TOTEM POLE OUTPUT CURRENT:  $\pm 400\text{mA}$
- DIP8/SO8 PACKAGES

### DESCRIPTION

L6561 is the improved version of the L6560 standard Power Factor Corrector. Fully compatible with the standard version, it has a superior performant multiplier making the device capable of working in wide input voltage range applications (from 85V to 265V) with an excellent THD. Furthermore the start up current has been reduced at few tens of  $\mu\text{A}$  and a disable function has been implemented on the ZCD pin, guaranteeing lower current consumption in stand by mode.

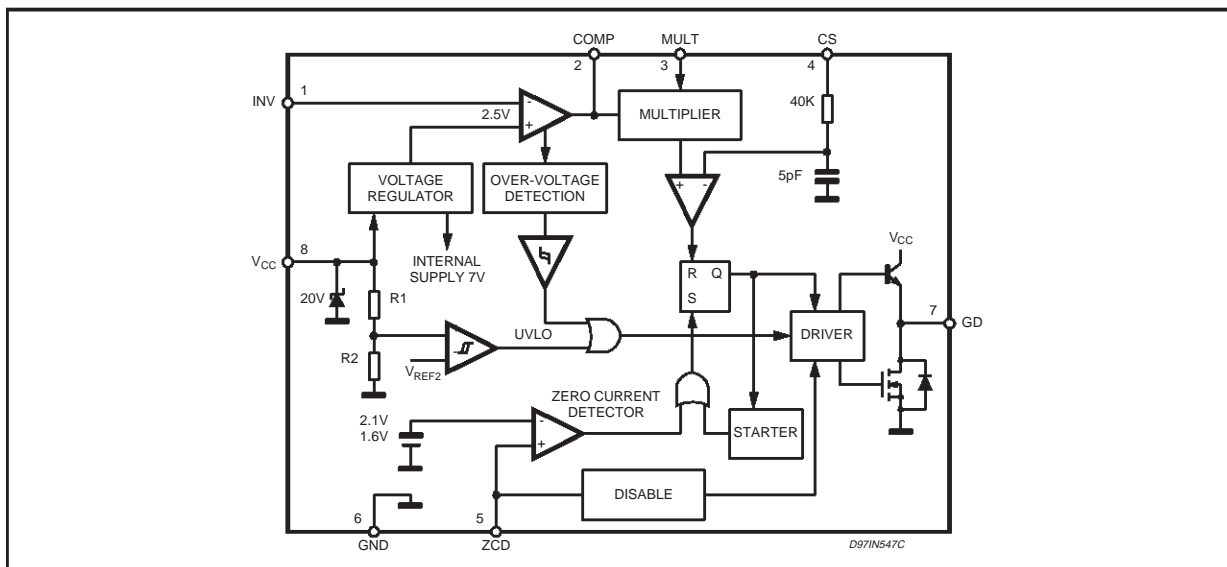


Realised in mixed BCD technology, the chip gives the following benefits:

- **micro power start up current**
- **1% precision internal reference voltage ( $T_j = 25^\circ\text{C}$ )**
- **Soft Output Over Voltage Protection**
- **no need for external low pass filter on the current sense**
- **very low operating quiescent current minimises power dissipation**

The totem pole output stage is capable of driving a Power MOS or IGBT with source and sink currents of  $\pm 400\text{mA}$ . The device is operating in transition mode and it is optimised for Electronic Lamp Ballast application, AC-DC adaptors and SMPS.

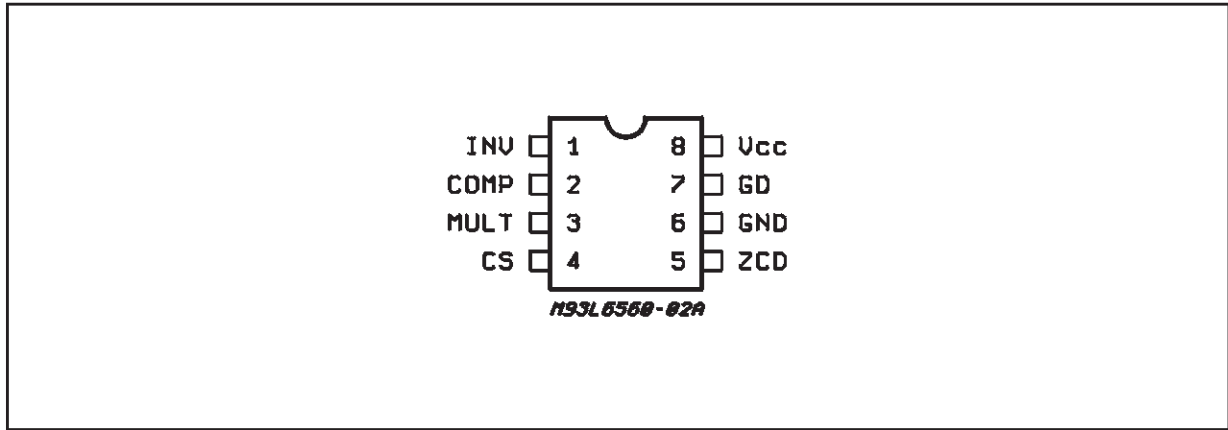
### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Pin	Parameter	Value	Unit
I <sub>VCC</sub>	8	I <sub>CC</sub> + I <sub>Z</sub>	30	mA
I <sub>GD</sub>	7	Output Totem Pole Peak Current (2μs)	±700	mA
INV, COMP MULT	1, 2, 3	Analog Inputs & Outputs	-0.3 to 7	V
CS	4	Current Sense Input	-0.3 to 7	V
ZCD	5	Zero Current Detector	50 (source) -10 (sink)	mA mA
P <sub>tot</sub>		Power Dissipation @T <sub>amb</sub> = 50 °C <b>(Minidip) (SO8)</b>	1 0.65	W
T <sub>j</sub>		Junction Temperature Operating Range	-40 to 150	°C
T <sub>stg</sub>		Storage Temperature	-55 to 150	°C

**PIN CONNECTION**



**THERMAL DATA**

Symbol	Parameter	SO 8	MINIDIP	Unit
R <sub>th j-amb</sub>	Thermal Resistance Junction-ambient	150	100	°C/W

**PIN FUNCTIONS**

N.	Name	Function
1	INV	Inverting input of the error amplifier. A resistive divider is connected between the output regulated voltage and this point, to provide voltage feedback.
2	COMP	Output of error amplifier. A feedback compensation network is placed between this pin and the INV pin.
3	MULT	Input of the multiplier stage. A resistive divider connects to this pin the rectified mains. A voltage signal, proportional to the rectified mains, appears on this pin.
4	CS	Input to the comparator of the control loop. The current is sensed by a resistor and the resulting voltage is applied to this pin.
5	ZCD	Zero current detection input. If it is connected to GND, the device is disabled.
6	GND	Current return for driver and control circuits.
7	GD	Gate driver output. A push pull output stage is able to drive the Power MOS with peak current of 400mA (source and sink).
8	V <sub>CC</sub>	Supply voltage of driver and control circuits.

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 14.5V$ ;  $T_{amb} = -25^{\circ}C$  to  $125^{\circ}C$ ; unless otherwise specified)  
**SUPPLY VOLTAGE SECTION**

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{CC}$	8	Operating Range	after turn-on	11		18	V
$V_{CC\ ON}$	8	Turn-on Threshold		11	12	13	V
$V_{CC\ OFF}$	8	Turn-off Threshold		8.7	9.5	10.3	V
Hys	8	Hysteresis		2.2	2.5	2.8	V

**SUPPLY CURRENT SECTION**

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{START-U}$	8	Start-up Current	before turn-on ( $V_{CC} = 11V$ )	20	50	90	$\mu A$
$I_q$	8	Quiescent Current			2.6	4	mA
$I_{CC}$		Operating Supply Current	$C_L = 1nF @ 70KHz$ in OVP condition $V_{pin1} = 2.7V$		4	5.5	mA
$I_q$		Quiescent Current	$V_{PIN5} \leq 150mV, V_{CC} > V_{CC\ off}$		1.4	2.1	mA
		Quiescent Current	$V_{PIN5} \leq 150mV, V_{CC} < V_{CC\ off}$	20	50	90	$\mu A$
$V_Z$	8	Zener Voltage	$I_{CC} = 25mA$	18	20	22	V

**ERROR AMPLIFIER SECTION**

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{INV}$	1	Voltage Feedback Input Threshold	$T_{amb} = 25^{\circ}C$	2.465	2.5	2.535	V
			$12V < V_{CC} < 18V$	2.44		2.56	
		Line Regulation	$V_{CC} = 12$ to $18V$		2	5	mV
$I_{INV}$	1	Input Bias Current			-0.1	-1	$\mu A$
$G_V$		Voltage Gain	Open loop	60	80		dB
GB		Gain Bandwidth			1		MHz
$I_{COMP}$	2	Source Current	$V_{COMP} = 4V, V_{INV} = 2.4V$	-2	-4	-8	mA
		Sink Current	$V_{COMP} = 4V, V_{INV} = 2.6V$	2.5	4.5		mA
$V_{COMP}$	2	Upper Clamp Voltage	$I_{SOURCE} = 0.5mA$		5.8		V
		Lower Clamp Voltage	$I_{SINK} = 0.5mA$		2.25		V

**MULTIPLIER SECTION**

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{MULT}$	3	Linear Operating Voltage		0 to 3	0 to 3.5		V
$\frac{\Delta V_{CS}}{\Delta V_{mult}}$		Output Max. Slope	$V_{MULT} =$ from $0V$ to $0.5V$ $V_{COMP} =$ Upper Clamp Voltage	1.65	1.9		
K		Gain	$V_{MULT} = 1V, V_{COMP} = 4V$	0.45	0.6	0.75	1/V

**CURRENT SENSE COMPARATOR**

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{CS}$	4	Current Sense Reference Clamp	$V_{MULT} = 2.5V$ $V_{COMP} =$ Upper Clamp Voltage	1.6	1.7	1.8	V
$I_{CS}$	4	Input Bias Current	$V_{OS} = 0$		-0.05	-1	$\mu A$
$t_d (H-L)$	4	Delay to Output			200	450	ns
	4	Current Sense Offset			0	15	mV

## ELECTRICAL CHARACTERISTICS (continued)

## ZERO CURRENT DETECTOR

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V <sub>ZCD</sub>	5	Input Threshold Voltage Rising Edge	(1)		2.1		V
		Hysteresis	(1)	0.3	0.5	0.7	V
V <sub>ZCD</sub>	5	Upper Clamp Voltage	I <sub>ZCD</sub> = 20μA	4.5	5.1	5.9	V
V <sub>ZCD</sub>	5	Upper Clamp Voltage	I <sub>ZCD</sub> = 3mA	4.7	5.2	6.1	V
V <sub>ZCD</sub>	5	Lower Clamp Voltage	I <sub>ZCD</sub> = -3mA	0.3	0.65	1	V
I <sub>ZCD</sub>	5	Sink Bias Current	1V ≤ V <sub>ZCD</sub> ≤ 4.5V		2		μA
I <sub>ZCD</sub>	5	Source Current Capability		-3		-10	mA
I <sub>ZCD</sub>	5	Sink Current Capability		3		10	mA
V <sub>DIS</sub>	5	Disable threshold		150	200	250	mV
I <sub>ZCD</sub>	5	Restart Current After Disable	V <sub>ZCD</sub> < V <sub>dis</sub> ; V <sub>CC</sub> > V <sub>CCOFF</sub>	-100	-200	-300	μA

## OUTPUT SECTION

V <sub>GD</sub>	7	Dropout Voltage	I <sub>GDsource</sub> = 200mA		1.2	2	V
			I <sub>GDsource</sub> = 20mA		0.7	1	V
			I <sub>GDsink</sub> = 200mA			1.5	V
			I <sub>GDsink</sub> = 20mA			0.3	V
t <sub>r</sub>	7	Output Voltage Rise Time	CL = 1nF		40	100	ns
t <sub>f</sub>	7	Output Voltage Fall Time	CL = 1nF		40	100	ns
I <sub>GD off</sub>	7	I <sub>GD</sub> Sink Current	V <sub>CC</sub> = 3.5V V <sub>GD</sub> = 1V	5	10	-	mA

## OUTPUT OVERVOLTAGE SECTION

I <sub>OVP</sub>	2	OVP Triggering Current		35	40	45	μA
		Static OVP Threshold		2.1	2.25	2.4	V

## RESTART TIMER

t <sub>START</sub>		Start Timer		70	150	400	μs
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(1) Parameter guaranteed by design, not tested in production.

## OVER VOLTAGE PROTECTION OVP

The output voltage is expected to be kept by the operation of the PFC circuit close to its nominal value. This is set by the ratio of the two external resistors R<sub>1</sub> and R<sub>2</sub> (see fig. 2), taking into consideration that the non inverting input of the error amplifier is biased inside the L6561 at 2.5V.

In steady state conditions, the current through R<sub>1</sub> and R<sub>2</sub> is:

$$I_{R1sc} = \frac{V_{out} - 2.5}{R1} = I_{R2} = \frac{2.5V}{R2}$$

and, if the external compensation network is made only with a capacitor C<sub>comp</sub>, the current through C<sub>comp</sub> equals zero.

When the output voltage increases abruptly the current through R<sub>1</sub> becomes:

$$I_{R1} = \frac{V_{outsc} + \Delta V_{OUT} - 2.5}{R1} = I_{R1sc} + \Delta I_{R1}$$

Since the current through R<sub>2</sub> does not change, ΔI<sub>R1</sub> must flow through the capacitor C<sub>comp</sub> and enter the error amplifier.

This current is monitored inside the L6561 and when reaches about 37μA the output voltage of the multiplier is forced to decrease, thus reducing the energy drawn from the mains. If the current exceeds 40μA, the OVP protection is triggered (Dynamic OVP), and the external power transistor is switched off until the current falls approximately below 10μA.

However, if the overvoltage persists, an internal comparator (Static OVP) confirms the OVP condition keeping the external power switch turned off (see fig. 1).

Finally, the overvoltage that triggers the OVP function is:

$$\Delta V_{out} = R1 \cdot 40\mu A.$$

Typical values for R<sub>1</sub>, R<sub>2</sub> and C are shown in the application circuits. The overvoltage can be set independently from the average output voltage. The precision in setting the overvoltage threshold is 7% of

the overvoltage value (for instance  $\Delta V = 60V \pm 4.2V$ ).

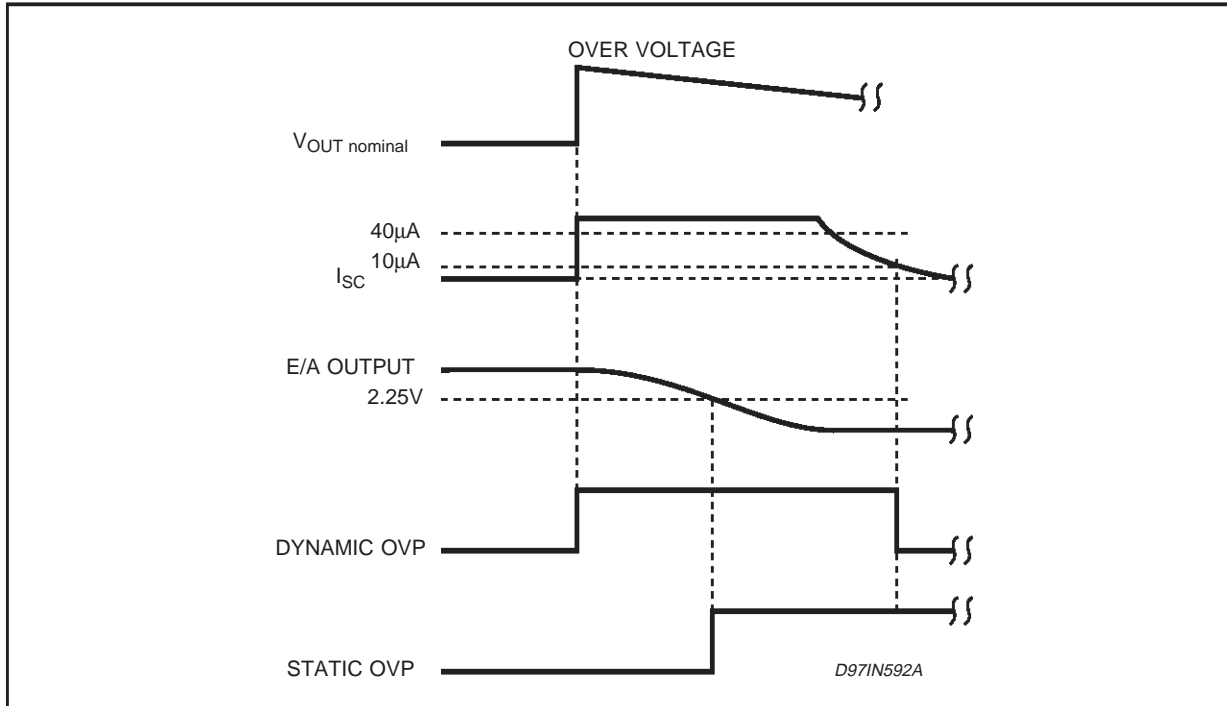
**Disable function**

The zero current detector (ZCD) pin can be used

for device disabling as well. By grounding the ZCD voltage the device is disabled reducing the supply current consumption at 1.4mA typical (@ 14.5V supply voltage).

Releasing the ZCD pin the internal start-up timer will restart the device.

**Figure 1.**



**Figure 2. Overvoltage Protection Circuit**

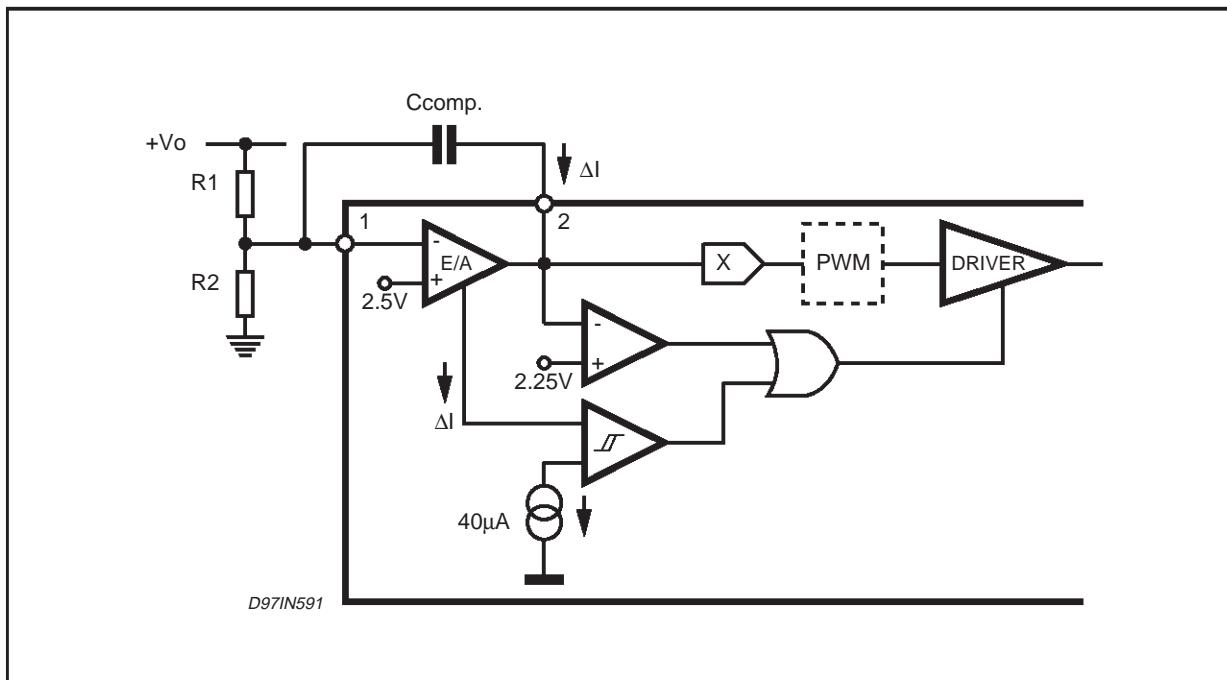


Figure 3. Typical Application Circuit (80W, 110VAC)

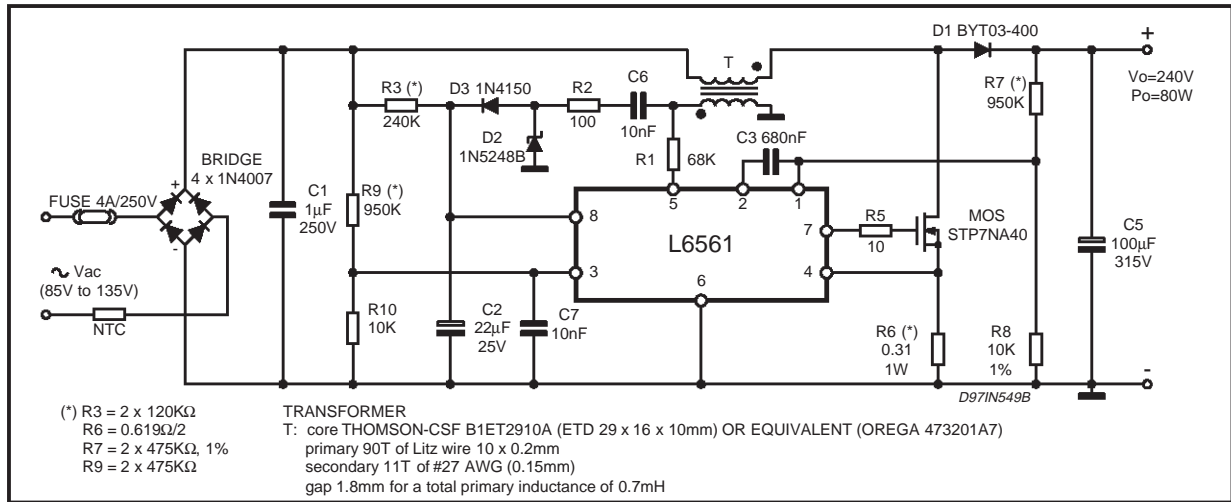


Figure 4. Typical Application Circuit (120W, 220VAC)

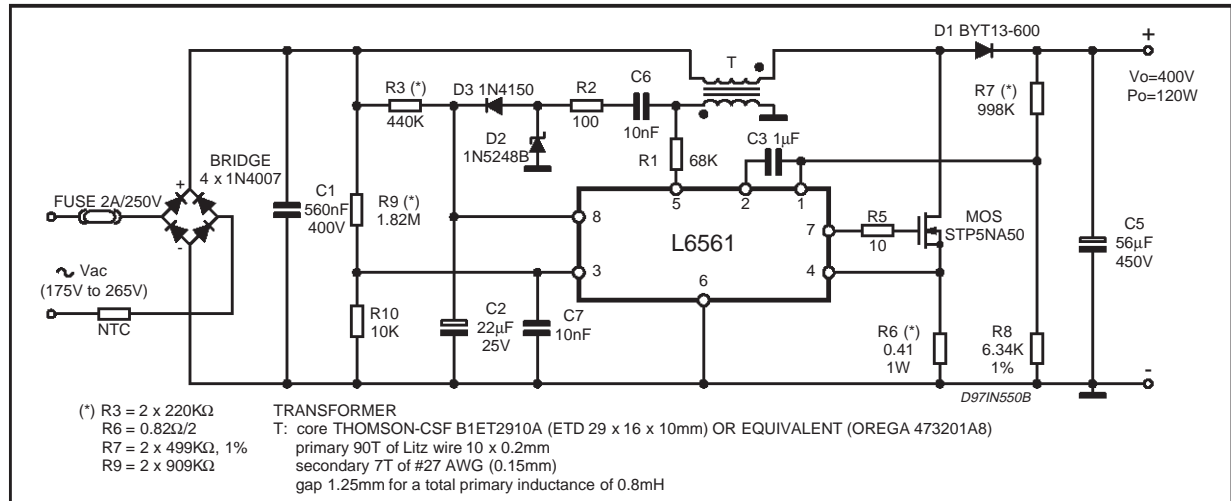


Figure 5. Wide-Range Application (80W)

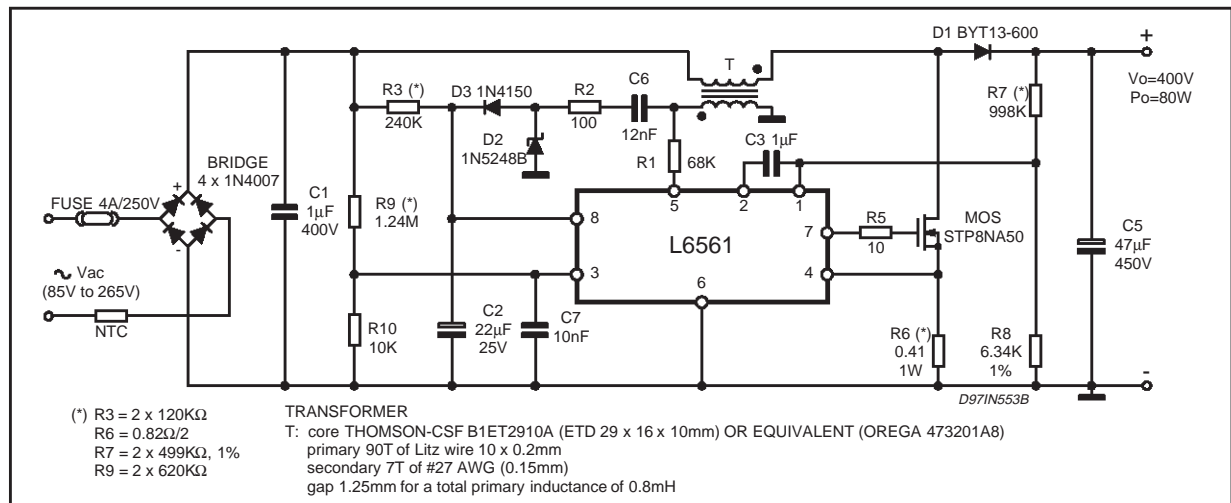


Figure 6. P.C. Board and Components Layout of the Fig. 3, 4 and 5 (1:1.25 scale)

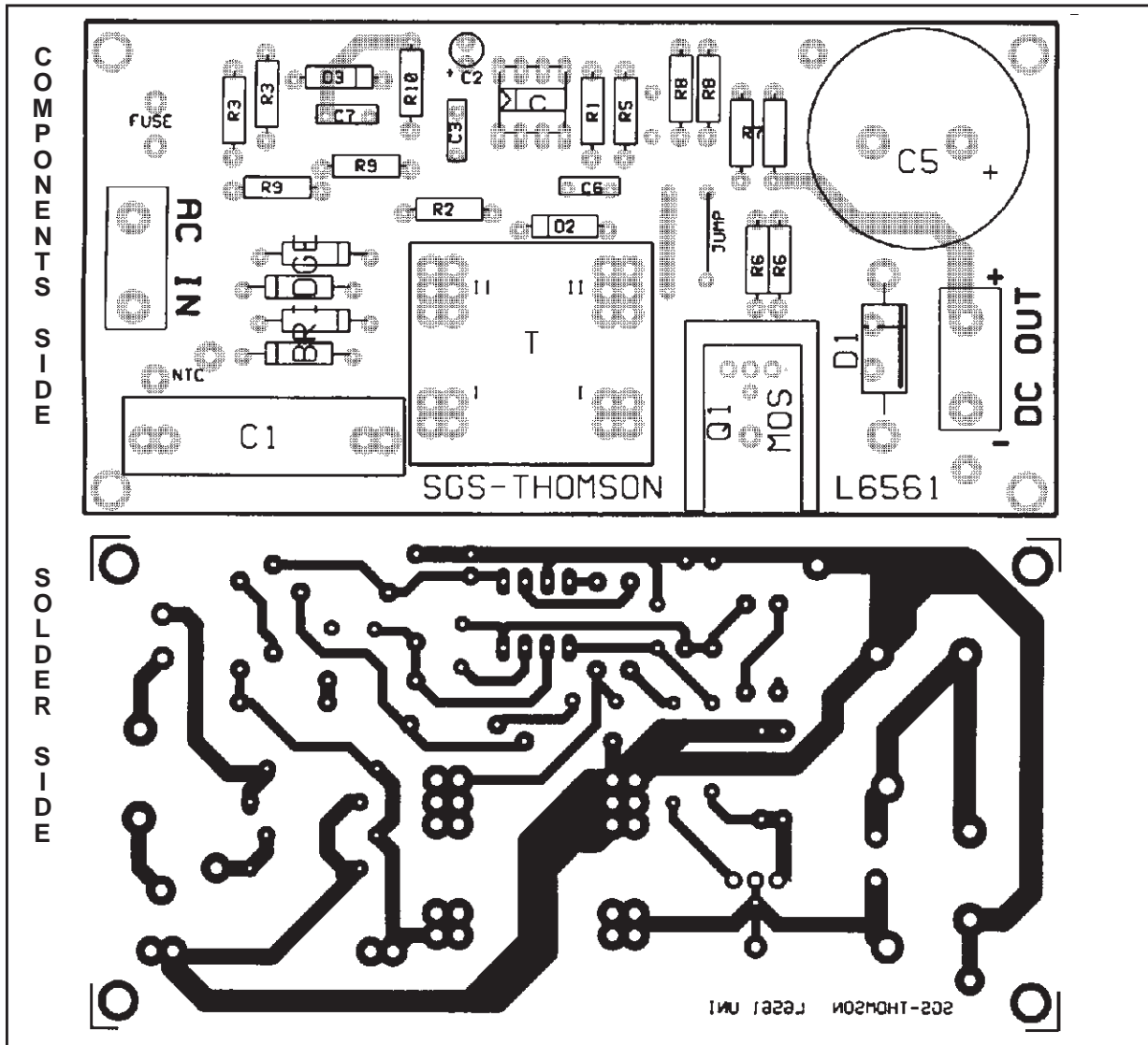


Figure 7. OVP Current Threshold vs. Temperature

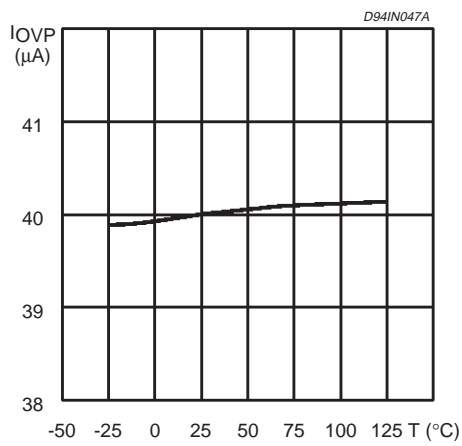


Figure 8. Undervoltage Lockout Threshold vs. Temperature

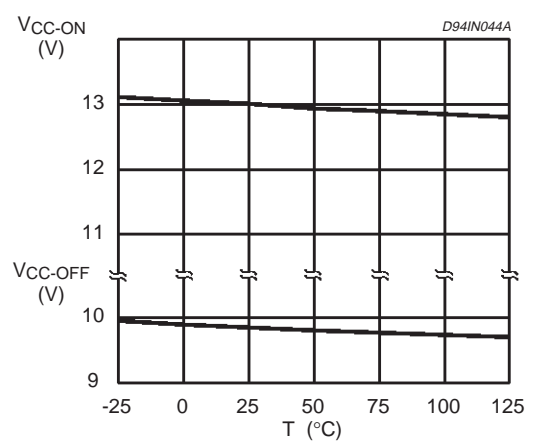


Figure 9. Supply Current vs. Supply Voltage

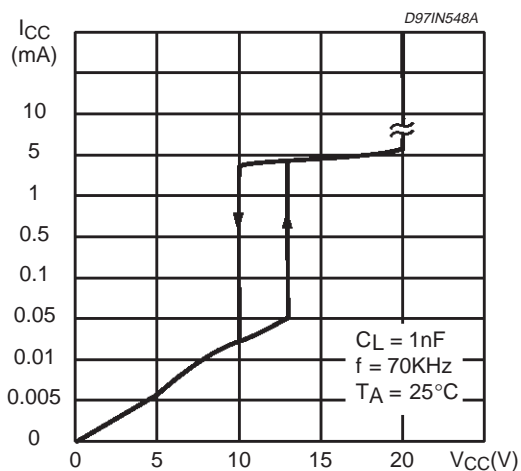


Figure 10. Voltage Feedback Input Threshold vs. Temperature

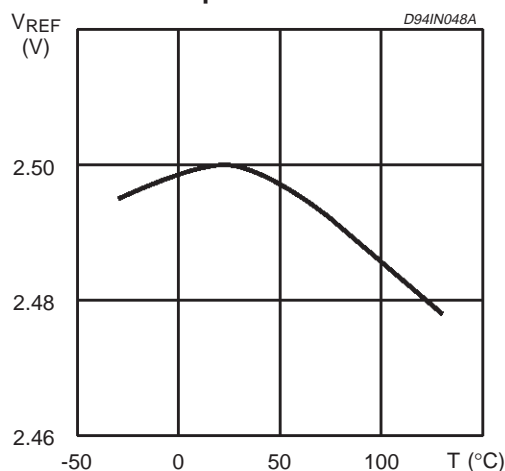


Figure 11. Output Saturation Voltage vs. Sink Current

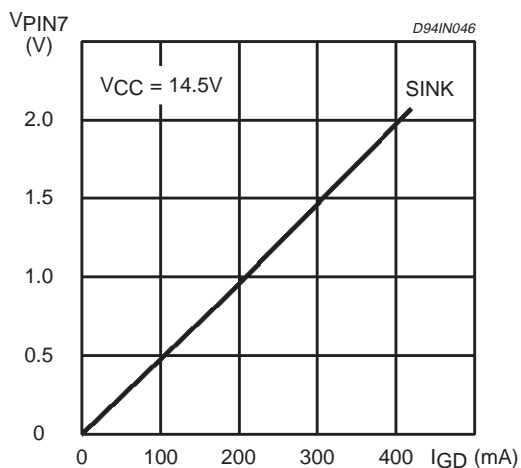


Figure 12. Output Saturation Voltage vs. Source Current

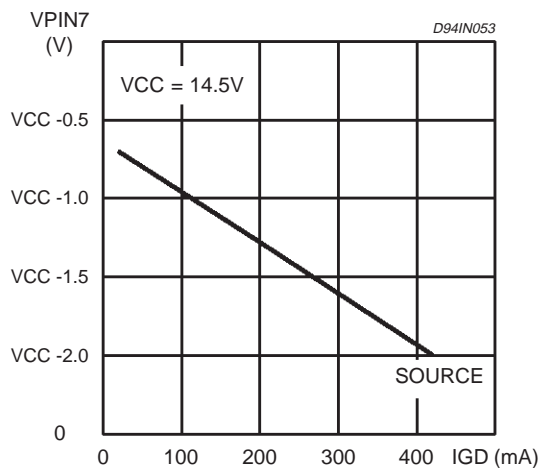
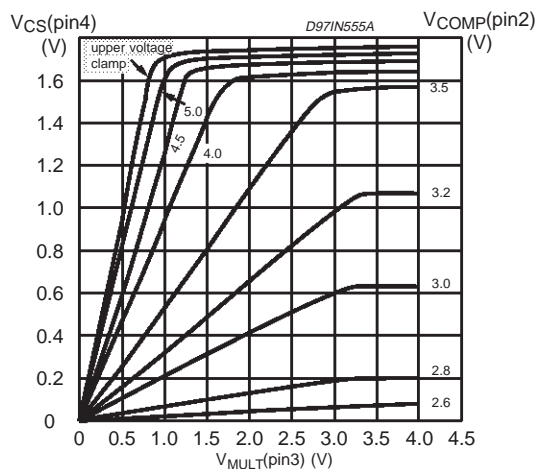


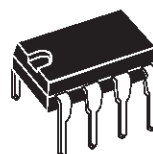
Figure 13. Multiplier Characteristics Family



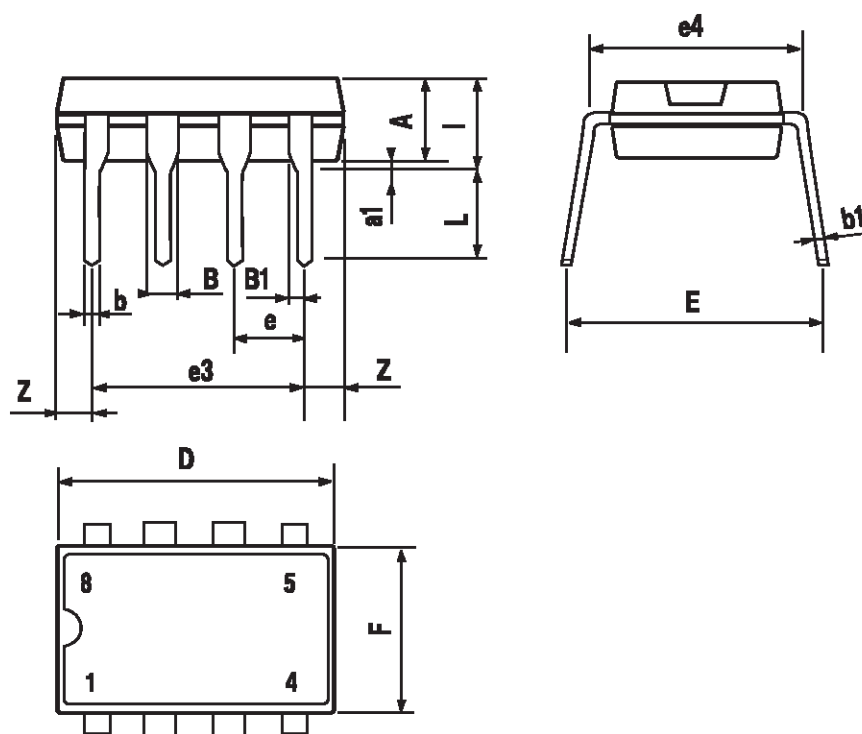


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

## OUTLINE AND MECHANICAL DATA

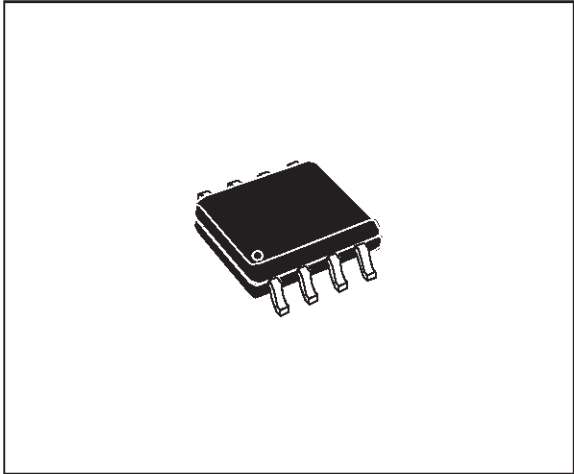


### Minidip



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

**OUTLINE AND MECHANICAL DATA**



**SO8**

(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).

